REMARKS

This communication is in response to the Official Action mailed November 27, 2002. Claims 1-20 were examined and are still pending. The Examiner rejected claims 1-3, 8, 18, and 19 under 35 U.S.C. §112, second paragraph. The Examiner also rejected claims 1-4, 7, and 18 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,363,509 (hereinafter "Parulkar et al"). Furthermore, the Examiner rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over Parulkar et al in view of U.S. Patent No. 6,370,494 (hereinafter "Mizuno et al").

The Examiner mentioned that claims 5, 6, and 20 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112, second paragraph. Finally, the Examiner allowed claims 9-17.

Applicant reviewed the Official Action, Parulkar et al, Mizuno et al, and the other cited references. Applicant amends claims * to further clarify the invention. Applicant also cancels claims * without prejudice. For reasons set forth below, Applicant requests reconsideration of this application.

Amendment to the Drawing

Applicant acknowledges the draft person's objections to the drawings. Appropriate correction will be made after allowance of this patent application.

Rejection Under 35 U.S.C. 112, P2 of Claims 1-3, 8, 18, and 19

The Examiner stated that claims 1-3, 8, 18, and 19 are rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting essential structural cooperative elements. Applicant has amended claims 1-3, 8, 18, and 19 to address the Examiner's objections.

In light of the amendment of claims 1-3, 8, 18, and 19 and the discussion below, Applicant requests that the rejection of these claims under 35 U.S.C. §112, second paragraph be withdrawn. Claims 1-3, 8, 18, and 19 are allowable.

Rejection Under 35 U.S.C. §102(e) of Claims 1-4, 7, and 18

The Examiner rejected Applicant's claims 1-4, 7, and 18 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,363,509 (hereinafter "Parulkar et al"). Applicant respectfully traverses.

Parulkar et al appears to do the exact opposite of the present invention as recited in claim 1. It uses a software simulator to generate the full VCD file for the whole design and for the full time window first. It then extracts a subsection of the software-generated VCD to test a sub-block of the actual hardware (not merely a hardware model) on the tester for a time window. Parulkar et al's sole purpose appears to be the automatic generation of test patterns (test vectors) and test sequencing data (referring to Parulkar et al's FIG. 2, his device 302 generates test patterns 318 and test sequencing data 319) to test his hardware system by converting software

simulation test data. In other words, Parulkar converted FROM the software simulation test data TO the hardware compatible hardware test data.

In contrast, amended claim 1 reads, in part:

> 1. (Amended) A method of creating a simulation history for a selected simulation session range for a hardware modeled design on demand, comprising steps:
> generating a value change dump (VCD) file by dumping state information from the hardware modeled design for the selected simulation target range. (emphasis added)

As discussed in the patent specification, one embodiment of the present invention as recited in claim 1 creates the VCD file in a manner that is opposite of Parulkar et al. In the present invention, the hardware model is used to capture the input vectors. In essence, the present invention takes a snap-shot of the hardware states. The hardware state information is dumped to the software simulator to create a VCD file. The VCD information is created from the hardware to the software, whereas in Parulkar et al, the VCD is created from the software to the hardware.

Amended claim 2 recites, in part:

> 2. (Amended) The method of claim 1, further comprising steps:
> providing primary inputs to the hardware modeled design for evaluation; and
> recording a simulation history for the simulation session range. (emphasis added)

As recited in amended claim 2, the inputs are provided to the hardware modeled design and the simulation history is recorded. Thus, the hardware emulator (and therefore, the hardware model) takes the inputs, evaluates them, and the evaluated output (among other data) are provided to the software simulator to generate the VCD file.

In contrast, Parulkar et al does not deal with the hardware model. It uses an actual hardware device that was manufactured after the design stage. Parulkar et al's system is limited because it doesn't generate intermediate hardware models like the present invention. Parulkar et al deals with an actual hardware system (e.g., a real chip) that were outsourced by chip makers according to design specifications to be tested in a real tester. In addition, Parulkar et al does not need inputs to the hardware to generate the VCD file. Rather, it takes software test data and automatically converts them to hardware-usable test patterns for use by the actual hardware device in a real tester.

Because dependent claims 3-4 and 7 incorporate the same limitations in independent claim 1 and dependent claim 2, the same arguments can be made to distinguish them from Parulkar et al. Also, independent and amended claim 18 incorporates similar language as claim 1 and thus, the same arguments can be made to distinguish it from Parulkar et al.

Accordingly, Applicant respectfully requests the allowance of claims 1-4, 7, and 18 over Parulkar et al in view of the above arguments.

Rejection Under 35 U.S.C. §103 of Claim 8

The Examiner rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over Parulkar et al in view of U.S. Patent No. 6,370,494 (hereinafter "Mizuno et al"). Applicant respectfully traverses.

Amended claim 8 recites, in part:

> 8. (Amended) The method of claim 21, further comprising steps:
> saving state information of the modeled design at simulation time t0 in a first file; and
> saving state information of the modeled design at simulation time t3 in a second file.

First and foremost, Parulkar et al should not be used as relevant prior art against claim 8. The relevant inquiry in determining whether a particular reference should be used against the claimed invention is the relationship between the problem which the inventor was attempting to solve and the problem to which any reference is directed.

Parulkar et al was concerned with somehow addressing the problem of the "lack of cooperation between designer and production test engineers, together with these fundamental differences between design and production testing environments, mak[ing] production testing even more difficult." (Parulkar et al, Col. 5, lines 53-57) Designers use software simulation with software-generated stimuli to test their design. When the design is reduced to a real physical chip, production test engineers get involved. However, the test stimuli they use with real testers are test patterns (test vectors) that are distinct from the stimuli used during the software simulation stage by the designers. Parulkar et al solved the problem by inventing an automatic converter for converting software test data to hardware-usable test data. By doing so, production test engineers can test real chips with their real testers with hardware-usable test data without having to handcraft the test patterns themselves.

The embodiments of the present invention, as recited in the claims, are not concerned with this design-production environment cycle. The present invention is concerned about how to restore the design state at any given simulation period range from the hardware model. The present invention facilitates the acceleration of the design process by allowing designers to reduce his design into a hardware model for testing. The state information in the hardware model is used to generate the VCD file for further use. The software stimuli is not used at all to test the hardware because the present invention does not care about the software stimuli. It uses the hardware states instead to debug in the software. The process is reversed.

Furthermore, unlike Parulkar et al, the present invention does not use an actual and real hardware chip manufactured by some vendor. The hardware model in the present invention is configured by the FPGAs to model the circuit design.

Accordingly, Parulkar et al is not relevant to the present invention in an obviousness determination. A person of ordinary skill in the art would not seek a solution to the problems mentioned in the present application because he would have no expectation of finding an appropriate teaching in Parulkar et al. Assuming, arguendo, that Parulkar et al is relevant, the

arguments made above by Applicant for claims 1 and 2 are relevant here for claim 8, which incorporates claim elements from claim 1.

The Examiner argues that Mizuno et al teaches saving state information of the modeled design in a second file, citing Mizuno et al, Col. 10, lines 25-28. The Examiner is mistaken. In this section of Mizuno et al, the device is not loading the simulation state (flip flops, latches, and memories); rather, it is loading the collected event count status. Mizuno et al states it as "all the operational statuses of the LSI that is being simulated are backed up."

In contrast, the embodiments of the present invention as recited in the claims and in particular, claim 8, restores the design state on demand. They do not count nor save event activity at all.

Accordingly, Applicant requests the Examiner to remove the 35 U.S.C. §103(a) rejection of claim 8 as being unpatentable over Parulkar et al in view of Mizuno et al. Applicant respectfully requests the allowance of claim 8.

CONCLUSION

Applicant has explained and clarified the patentability of the present invention, as recited in claims 1-22. First, Applicant requests that the Examiner withdraw the 35 U.S.C. §112, second paragraph rejection of claims 1-3, 8, 18, and 19. Second, Applicant has pointed out the novelty and distinction of the present invention to overcome the Examiner's 35 U.S.C. §102(e) rejection of claims 1-4, 7, and 18 as being anticipated by Parulkar et al. Finally, Applicant has pointed out the nonobviousness of the present invention to overcome the Examiner's 35 U.S.C. §103(a) rejection of claim 8 over Parulkar et al and Mizuno et al. The Examiner allowed claims 9-17.

Accordingly, in view of the above remarks, Applicant submits that this application is now ready for allowance. Early notice to this effect is solicited.

If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (650) 320-4104.

Respectfully submitted,

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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited on February 27, 2003, with the U.S. Postal Service as First class mail in an envelope addressed to: Box Fee Amendment, Assistant Commissioner for Patents, Washington, D.C., 20231.

Date: February 27, 2003

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